Specification Amendments

Please replace paragraph 007 as follows:

0007 Typically, in a dual damascene manufacturing process known in the art as a via-first-trench last process conventional photolithographic processes using a photoresist layer ~~is~~ are first used to pattern and expose an etching mask which is used for etching via openings through the IMD layer. Subsequently a similar process is used to define trench openings that are formed substantially over the via openings which in turn define metallic interconnect lines. ~~t~~The via openings and trench openings are subsequently filled with metal to form metalization vias and metal interconnect lines. The surface may then be planarized by conventional techniques to better define the metal interconnect lines and prepare the substrate for further processing.

Please replace paragraph 008 as follows:

0008 During the photolithography process, undercutting the photoresist layer acts to decrease the spacing between metallic lines[,] and compromises device design. As an example of compromised electrical property functionality, the distance between metal interconnect lines may be decreased such that

leakage current by a tunneling mechanism may occur. Further, undercutting the photoresist layer acts to weaken the mechanical integrity of the remaining photoresist lines, thereby increasing the possibility of photoresist line failure. In addition, even if the photoresist line doesn't fail, a dielectric insulating material made thinner as a result of undercutting may be structurally weakened and may lead to insulation failure in a resulting semiconductor device. In any case, the integrity of subsequent steps in the dual damascene process are compromised.

Please replace paragraph 0010 as follows:

0010 Typically, an antireflectance coating (ARC) layer 15 may be formed over the etching stop layer 14 prior to the conventional photolithographic process used for patterning the via openings 12a, 12b. The ARC layer 15 reduces the effect of light reflection undesirably exposing a photoresist overlayer 16 used for defining via openings 12a, 12b. Light reflection (scattering) from, for example, the IMD layer 10 surface, etching stop layer 14 surface, and their respective interfaces, can cause undesired light exposure of an overlying photoresist layer 16 in a photolithographic masking and patterning steps, for example, in the formation of via openings 12a, 12b. As a result, upon

development and removal of the exposed photoresist the phenomenon of undercutting (removing photoresist exposed by reflected light in the foot area of the photoresist) will detrimentally affect the design integrity of the manufactured device.

Please replace paragraph 0015 as follows:

0015 One solution to the problem of undercutting would be to increase the distance between the trench line patterns or decrease the metal line thickness thereby lessening any mechanical weakening effect due to undercutting. Neither of these proposed solutions, however, are compatible with the trend and necessity of continually scaling down structure size. Another solution would be to apply an ARC layer in such a way to avoid the effect of undesired light scattering and reflections from via edges and sidewalls.

Please replace the paragraph 0042 as follows:

0042 The photoresist layer ~~36~~ 37 serving to define the trench opening pattern ~~38~~ 39 is preferably from ~~5000 to 9000~~ 1000 to 20000 Angstroms. It will further be appreciated by those skilled in the art that positive photoresist is the preferable photoresist.